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LOW POWER SRAM DESIGNS: A REVIEW

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ABSTRACT

With on growing technology scaling, low power operation has become important in VLSI design. SRAM consists large portion of the modern VLSI designs, thus efforts are being made to design low power SRAM using different ways. This paper discusses various existing SRAM designs, consisting of different number of transistors from one another. This paper focuses on the study of these designs and their comparison on the basis of parameters like power dissipation, access time , stability and power delay product. All the SRAM designs has different read write operation and hence different results. It was found that 12T SRAM has better performance in case of power dissipation and power dealy product but high access time than the other existing SRAM cells when compared on the basis of simulation results obtained on 45nm environment using Microwind tool.

KEYWORDS: SRAM; low power; static and dynamic power; leakage power; static noise margin; charge sharing; swing voltage.

INTRODUCTION

The requirement for low power high speed portable devices like cellular phones, computer laptops, notebook, etc. is increasing continuously. All these devices require primary memory that works and responds much faster and needs no refreshing. For that purpose SRAM (as cache memory) is used which acts as an important part of modern microprocessor design. SRAM occupies large portion of total chip area and power. Over 70% of the chip area is being occupied by SRAM due the increasing density of SRAM caches which provide an effective method to enhance system performance [1].

Unwanted power dissipation in SRAM in the form of dynamic and static power dissipation reduces the battery backup life of the portable devices. Thus decreasing the power dissipation of SRAM can lead to more efficient and fast IC'S. so it is required to have a SRAM cell design having low power dissipation. Many techniques have been introduced to fulfill this requirement such as scaling the supply voltage, using multi-threshold CMOS (MTCMOS) process, logic optimization, pipelining and parallelism etc.[2] As technology scales down not only the leakage power dissipation starts to increase but also has other negative impacts such as drain induced barrier lowering (DIBL), increased source to drain resistance etc.[3]

To achieve the low power SRAM cell various SRAM designs has been framed according to the need which started with the conventional 6T SRAM, having 6 number of transistors in it.

Initially the area and cost of chip were considered important factors but with growing technology, speed and power has dominated over previous thought.

This paper discusses various designs of SRAM with different number of transistors used. Each design has some improved factor as compared with other. Some of the designs have focused on decreasing the dynamic and static power, while as some have focused on increasing the stability of SRAM. This paper gives the brief information regarding various SRAM designs and compares them on the basis of power, delay, number of transistors used and power delay product.

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This paper is organized as follows: section 2 describes the different SRAM designs, section 3 discusses the comparison of cells on the basis of various parameters, section 4 describes the conclusion and future work.

DIFFERENT SRAM DESIGNS

Conventional 6T SRAM

Fig. 1 shows the circuit diagram of conventional 6T SRAM[4].this SRAM design is most simple and less area consumed design consists of two access transistors and two cross coupled inverters with common read and write port. During the write operation the WL is selected, access transistors are turned on, the value to the bit line and bit line bar is given and is stored at q and q-bar.

Before the read mode , the bit lines(BL) and bitbar line(BL bar) are precharged to as high as V_{dd} (supply voltage).when the word line is enabled, current will flow from V_{dd} through the pull up transistor TP1of the node storing 1. Simultaneously current will flow from precharged bitbar line to ground, thus discharging bitbar line. All this causes voltage difference between the bit lines, this voltage difference is detected and amplified with the help of any sense amplifiers at the data output.

ADVANTAGES: The SRAM design is simple, less area consumed and thus can be used in high density chips.
DISADVANTAGE: on voltage scaling, has less stability, has high power consumption and high access time.

6T single ended SRAM cell

Fig 2 shows the single ended 6T SRAM cell [5] consists of a cross coupled inverter pair INV1 and INV2 connected to bitline with the help of access transistor M5 and has an isolated transistor M6 as read port. Design also uses two assist transistors one used for memory write access (MWA) and other used for memory read access (MRA) purpose.

Write operation of this design is bit difficult because of strongly cross coupled inverters. During the write operation WWL is select high which turns access transistor M5 on and bit line is precharged with the value to be stored in the cell.

As both the inverters are strongly cross coupled forcing the node Q to store data is difficult. Hence memory write access transistor MWA is inserted in series with INV2 which is controlled by W0 to turn it off during the write operation, thus weakens the strongly cross coupled inverters.

Before read operation BL is precharged to V_{dd} and the read word line(RWL) is selected high, W0 is also selected high to turn on the transistor MRA for reading '0'. Reading '1' is not effected by MRA , thus is directly sensed from precharged BL.
ADVANTAGES: Read SNM of this design is more than standard 6T[5]. This design has 0.302V SNM, while the standard 6T SRAM design has 0.152V at supply voltage 1V. Also the power consumption in this cell is less than that of 6T SRAM.
DISADVANTAGES: 6T SRAM generally goes through severe stability issues as supply voltage is reduced. This issue becomes worse due to increased variability in below sub-100nm technology [6].

High stable, dual port, sub-threshold 7T SRAM cell for Ultra –low power application

Fig 3 shows the sub-threshold 7T SRAM cell [6], based on 90nm technology. It is sub-threshold 7 transistor based SRAM working on supply voltage of 0.17V.unlike 6T conventional SRAM it has single sided write operation. For the write operation word line (WL) is set high and write bit line is precharged with the data to be stored in the cell. Write bit line is precharged higher than the write margin of the cell to reduce dynamic power during write 1 operation.

Read path is separated from the storing node of the cell which increases noise margin. For reading the data, Read word line and Read bit both are set high. Transistors M6, M7 are used for reading the cell data. The connection of M7 transistor to virtual ground minimizes the standby leakage of the cell.

ADVANTAGES: This cell demonstrates 7X higher dynamic read noise margin compared to the 6T SRAM cell. Cell works well in sub-threshold region with low supply voltage as low as 0.17V [6].

DISADVANTAGE: This design has shown increase of area by almost 7% than the 6T SRAM.

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Novel 9T SRAM cell

Fig 4 shows novel 9T SRAM cell [7] which is simulated on 65nm technology. This design is proposed for simultaneously reducing leakage power and improving data stability. This design has two sub-circuits, one the upper sub-circuit which is simply 6T SRAM design but with minimum sized features. This sub-circuit is used for write operation. Lower sub-circuit consists of access transistors N5 and N6 and one read access transistor N7. Transistor N5 and N6 are controlled by data present on the node 1 and node 2 respectively. However transistor N7 is controlled by read signal RD.

For the write operation, WR signal is set high, turning the access transistors N3 and N4 ON, while RD set low thus maintaining N7 transistor in cut off mode. Bit lines are than precharged with the data and gets stored on node 1 and node2.

Read operation occurs separately through N5, N6 and N7. During this operation WR is set low while RD set high making transistor N7 in working mode. If node 1 stores '1', bit line is discharged through N5 and N7, and when bitbar line stores '1' it gets discharged through N6 and N7, causing in both the cases potential difference between the bitlines which is sensed and amplified by the sense amplifier during this read operation.N3 and N4 are cutoff, thus storage nodes node 1 and node 2 are completely isolated from the bitlines during read operation.

ADVANTAGES: The leakage power consumed by the 9T SRAM cell is 7.7% lower as compared to the standard 6T SRAM [7].

DISADVANTAGE: the area consumed by this design is more by 37.8% as compared to the conventional 6T SRAM cell and is slightly more than 7T SRAM cell [7].

P-P-N based 10T SRAM

Fig 5 shows novel P-P-N based 10T SRAM cell for low leakage and subthreshold operation [8]. This cell can operate at a voltage as low as 285mV[8]. The cell consists of two cross coupled P-P-N inverters. Transistors PUL1, PUL2 AND PDL2 form one P-P-N inverter and PUR1, PUR2, PDR2 form another, where PUL stands for pull-up-left ,PUR for pull up right, PUD for pull-down left and PDR for pull down right. Two more transistors pass gate left(PGL) and pass gate right(PGR) are the access transistors controlled by write line WL. For the read operation, discharging path is provided by additional transistors either PDL1 or PDR1. The source terminal of these two transistors is connected to VGND. Whenever the write operation is going VGND is set high to V_{dd} to curb unnecessary leakage current and only during read operation it is connected to ground, giving discharging path to one of the bitlines.

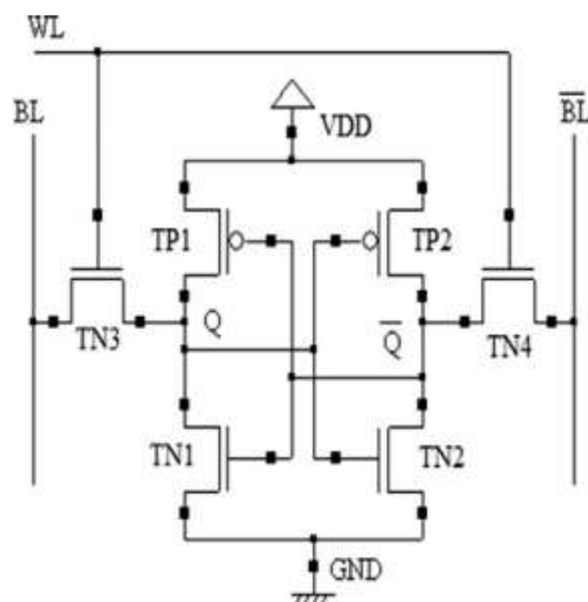

Fig 1.Conventional 6T SRAM cell

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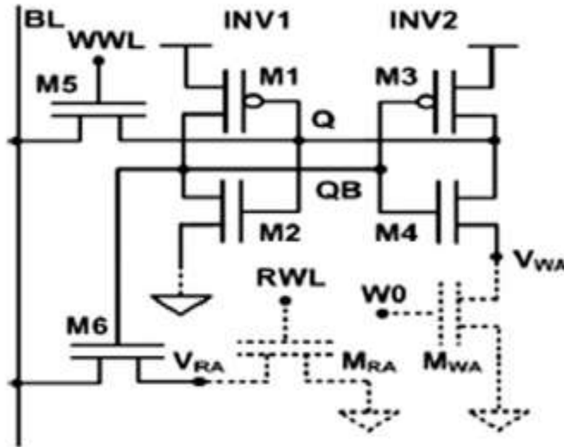

Fig 2. 6T single ended SRAM cell

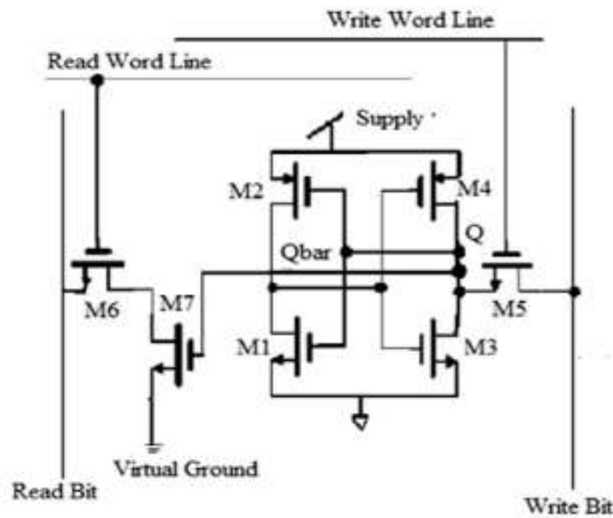

Fig 3. Subthreshold 7T SRAM Cell

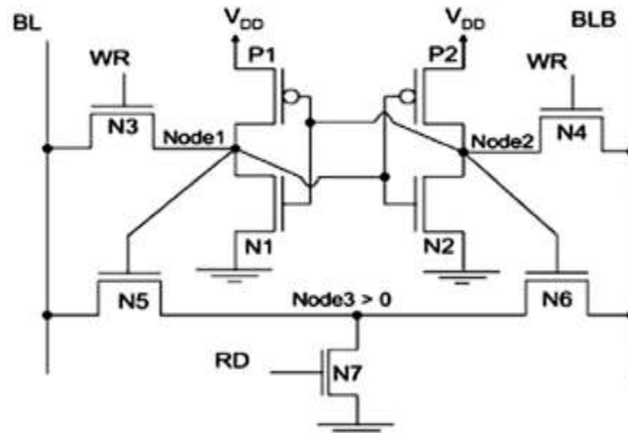

Fig 4.9T SRAM cell

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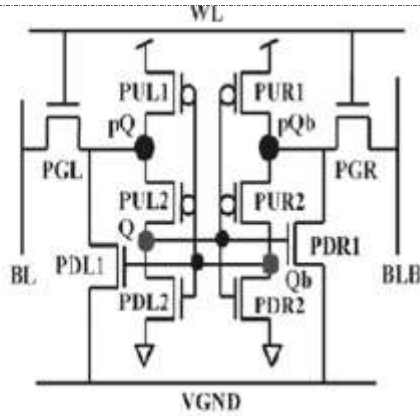

Fig 5. P-P-N based differential 10T SRAM

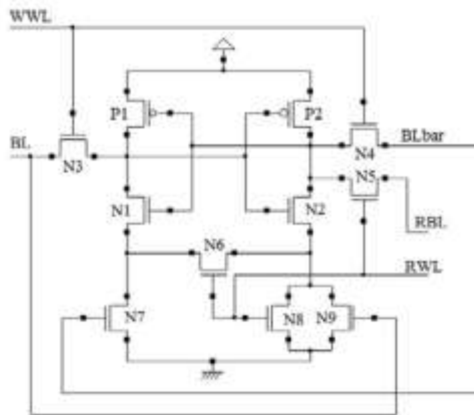

Fig 6. 11T SRAM cell

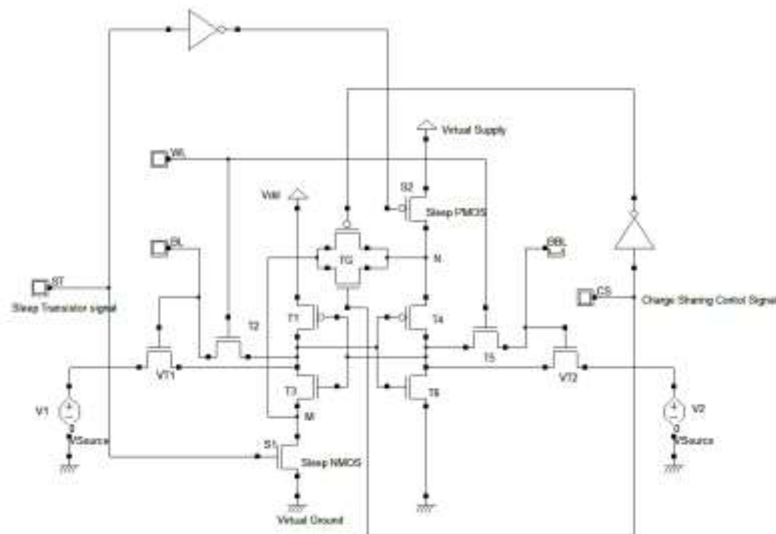

Fig 7. 12T SRAM

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Node PQ and pQb are called the pseudo storage nodes, both of them are in between the two cascaded PMOS's.The presence of these psedo nodes causes the isolation of the actual storing
nodes from the pair of bit lines which helps to reduce the data-dependent bitline leakage.
Rest of the write and read operation is same as that in the 6T SRAM cell design.

ADVANTAGES: this cell design has low power dissipation as compared to 6T SRAM also works better in sub threshold voltage as low as 285Mv[8]

DISADVANTAGE: the area covered by the cell is more as more no of transistors are being used in the design as compared to the 6T SRAM cell.

11T SRAM cell

Fig 6 shows low power 11T SRAM [9]. This design is proposed for low power consumption which has 11 numbers of transistors on 0.25 um technology with the help of tanner EDA tool. Basic storing cell of the design is same as that of 6T SRAM with transistors P1, P2, N1, N2, N3 and N4, where N3 and N4 are controlled by word line WWL. In addition to the 6T design there are two tail transistors N7and N9 which are controlled by bit line and bit bar line respectively. Another two transistors N8 and N6 are used for read operation. Transistor N5 is the access transistor for read operation which is driven by read word line RWL. Single bit-line RBL is used for read operation.

During write operation RWL is set low and WWL is select high thus turning access write transistors N3 and N4 on. Bit lines are precharged according to the data to be stored in the cell.

During read operation WWL=0 and RWL= high, thus turning transistor N6 and N8 on. Depending upon the stored data at node B, either read '0' or read '1' can be performed.

ADVANTAGES: The proposed design SRAM cell consumes approximately 40% less average power compared to conventional 6T SRAM design [9].

DISADVANTAGES: The proposed cell consumes more are than the 6T SRAM as well as this cell is almost 7% slower than the conventional cell during the write operation due to two tail transistors[9].

Low power 12T SRAM cell.

Fig 7 shows the design of low swing and multi threshold voltage based low power 12T SRAM [10]-[12]. This design is proposed mainly for the low power application and is simulated on 45 nm technology. The read and write operation of the cell is exactly the same as that of 6T SRAM. As it includes 6T SRAM along with some extra circuitry for low power dissipation in the design.
This design makes use of two voltage sources V1, connected to the bitline through transistor VT1 and V2, connected to the bitbar line through transistor VT2 which reduce the swing at the output node and thus reduce the dynamic power dissipation of the cell during the switching activity. Transistor VT1 and VT2 are controlled by data precharged to the bitline and bitbar line respectively. whenever the bitline ='1' and bitbar line ='0', transistor VT1 is turned on and VT1 turned off. Thus forcing the voltage swing to decrease at the output node of the bit line. Similarly for the write operation of '0' reverse case occurs and transistor VT2 is on thus voltage source V2 forces decrease of the swing voltage at node connected to bitbar line. Thus in both cases decreases the dynamic power of the cell.

As the design is making use of low V_t transistors (of inverter) therefore to reduce the power dissipation, MTCMOS technology by using the high Vt transistors S1(sleep NMOS) and S2(sleep PMOS) is used. where S1 connects the virtual ground i.e node M in fig 7 to the actual ground, whereas the S2 connects the virtual supply i.e node N to the actual V_{dd} supply. This technique reduces both leakage power in sleep mode of the cell as well the dynamic power.

This design also has another low power technique used in it i.e charge recycling technique. This technique reduces static power dissipation during switching between active and sleep modes of the circuit. This technique is used by employing a transmission gate TG between the virtual ground (M) and the virtual supply (N). TG is turned on just before switching from sleep to active or active to sleep mode during write operation, to balance the leakage power thus reducing the static power of the cell.

ADVANTAGE: This SRAM cell design has very less power and low power delay product (PDP) as compared to the 6T conventional SRAM cell as well as with that of other discussed SRAM designs [10].

DISADVANTAGE: The cell covers large area of the chip and has high access time as compared to the conventional 6T SRAM .

COMPARISON OF THE RESULTS

In this section all the discussed SRAM cells are being compared on the basis of power dissipation, access time and power delay product. These simulations are being done in 45nm environment with the help of Microwind 3.1 tool by using BSimM4 model. Table 1 and table 2 shows the comparison of SRAM cells on the basis of different parameters [10]:

CONCLUSION AND FUTURE WORK

In high speed SRAM cells stability, access time and power dissipation are the major issues. In this paper different SRAM designs have been discussed. All the designs are different from each other on the basis of number of transistors used and also on the basis of their read write structure. These designs differ not only in power dissipation but in access time, stability and power delay product also. The simulation results show that moving from 6T to 12T SRAM area increases but the power dissipation and power delay product improves when simulated on 45nm technology. Thus depending on the need, low power SRAM design can be used to provide low power solution in high speed devices like laptops, mobile phones, e.t.c.

In future moving from the 12 T SRAM design, there can be further improvements in the design for more low power applications. In 12T SRAM cell access transistors can be replaced by TG. By that better results can be obtained. Furthermore latch of 12T SRAM can be replaced by some low power latch which can further reduce leakage power of the cell.

Table 1. comparison of power dissipation

SRAM CELLS	Static power dissipation for write operation (µW)	Dyanamic power dissipation for write operation (µW)	Static power dissipation for read operation (µW)	Dynamic power dissipation for read operation (µw)
Conventional 6T SRAM[4]	6.263	9.234	7.731	6.967
6T single ended[5]	4.478	7.178	4.399	4.571
Subthreshold 7T[6]	3.119	6.374	3.293	5.171
9T SRAM cell[7]	6.117	7.901	5.992	7.901
PPN based differential 10T [8]	4.190	5.895	2.246	3.957
11T SRAM [9]	3.867	4.957	2.038	3.595
12T SRAM[10]	2.895	3.734	1.893	2.736

Table 2. comparison of access time and power delay product

SRAM CELLS	Write access time	Read access time	PDP during write operation	PDP during read operation

Conventional 6T SRAM[4]	5.3.1	7.672	$1.814e^{-18}$	$1.331e^{-19}$
6T single ended[5]	6.828	9.201	$1.492e^{-18}$	$1.034e^{-19}$
Subthreshold 7T[6]	10.033	14.611	$1.225e^{-18}$	$1.541e^{-19}$
9T SRAM cell[7]	12.644	16.633	$1.628e^{-18}$	$1.944e^{-19}$
PPN based differential 10T [8]	12.540	15.429	$0.956e^{-18}$	$1.241e^{-19}$
11T SRAM [9]	15.861	19.392	$0.829e^{-18}$	$0.738e^{-19}$
12T SRAM[10]	9.109	12.494	$0.6371e^{-18}$	$0.5721e^{-19}$

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